



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/614,363

07/12/2000

John M. Airey

15-4-632.51

2211

28393

7590

07/13/2004

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVE., N.W.
WASHINGTON, DC 20005

EXAMINER

HAVAN, THU THAO

ART UNIT

PAPER NUMBER

2672

24

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/614,363

Applicant(s)

AIREY ET AL.

Examiner

Thu-Thao Havan

Art Unit

2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-13,22,26-33 and 35-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-13,22,26-33 and 35-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claims 1-3,5-13,22,26-33 and 35-37 are pending in the present application.

Response to Arguments

Applicant's arguments filed April 29, 2004 have been fully considered but they are not persuasive. As addressed below, Rossin and Deering teach the claimed limitations.

Rossin discloses a floating point format and a floating point frame buffer coupled to the raster subsystem for storing a plurality of floating point color values (col. 2, lines 12-67). In other words, Rossin teaches the divider performs a floating point divide operation on a floating point numerator and a floating point denominator. The comparator performs a comparison of the floating point denominator, except for a sign bit of the floating point denominator, with a floating point value of 0.0. A logic element, responsive to a control signal indicative of the floating point divide operation, provides to the comparator equal sign bits associated with the floating point denominator and the floating point value of 0.0. A result of the comparison indicates a divide by zero operation and is independent of the sign of the floating point denominator. In that he teaches a storage device, such as a register file, for providing the floating point numerator and the floating point denominator to the divider, and for providing the floating point value of 0.0 and the floating point denominator to the comparator. A first register may be coupled between the register file and the comparator for holding the

floating point value of 0.0. A second register may be coupled between the register file and the comparator for holding the floating point denominator, except for the sign bit of the floating point denominator. The logic element may comprise an AND gate receiving the control signal at a first input and the sign bit of the floating point denominator at a second input.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim **31** is rejected under 35 U.S.C. 102(e) as being unpatentable by Rossin et al. (US Patent No. 5,862,066).

Re claim **31**, Rossin discloses a computer system comprising a raster subsystem for performing a rasterization process, the rasterization process performed in a floating point format and a floating point frame buffer coupled to the raster subsystem for storing a plurality of floating point color values (col. 2, lines 12-67). In other words, Rossin teaches a typical computer graphics system include a geometry accelerator, a rasterizer and a frame buffer. The output from the geometry accelerator, referred to as rendering data, is used by the rasterizer (and optional texture mapping hardware) to compute final screen space coordinates and R, G, B color values for each pixel constituting the primitives. The pixel data is stored in the frame buffer for display on a display screen.

In that the geometry accelerator may be required to perform on the order of hundreds of millions of floating point calculations per second per chip. Functions of the geometry accelerator may include three-dimensional transformation, lighting, clipping, and perspective divide operations as well as plane equation generation, performed in floating point format. Geometry accelerator functions result in rendering data which is sent to the frame buffer subsystem for rasterization.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **1-3, 5-13, 22, 26-30, 32-33, and 35-37** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rossin et al. (US Patent No. 5,862,066) in view of Deering et al. (US Patent No. 6,115,047).

Re claim **1**, Rossin teaches a rasterization circuit coupled to the processor that rasterizes the primitive according to a rasterization process which operates using a floating point format (col. 7, lines 18-41; col. 3, lines 1-19), a frame buffer coupled to the rasterization circuit for storing a plurality of image values in a floating point format and a display screen coupled to the frame buffer for displaying an image according to the image values stored in the frame buffer (col. 2, lines 12-67; col. 3, lines 20-32). In other words, Rossin teaches a typical computer graphics system include a geometry

Art Unit: 2672

accelerator, a rasterizer and a frame buffer. The output from the geometry accelerator, referred to as rendering data, is used by the rasterizer (and optional texture mapping hardware) to compute final screen space coordinates and R, G, B color values for each pixel constituting the primitives. The pixel data is stored in the frame buffer for display on a display screen. In that the geometry accelerator may be required to perform on the order of hundreds of millions of floating point calculations per second per chip.

Functions of the geometry accelerator may include three-dimensional transformation, lighting, clipping, and perspective divide operations as well as plane equation generation, performed in floating point format. Geometry accelerator functions result in rendering data which is sent to the frame buffer subsystem for rasterization.

However, Rossin fails to explicitly teach a processor for performing geometric calculations on a plurality of vertices of a primitive. On the other hand, Deering teaches a processor for performing geometric calculations on a plurality of vertices of a primitive (col. 10, line 60 to col. 11, line 63; figs. 7-8 and 11). He teaches the F-core processor receives geometry primitive data and performs floating point operations on the received geometry data. He discloses detailed surface geometry may be rendered using texture maps, although providing more realism requires raw geometry, usually in the form of triangle primitives. In modern workstation computer systems, position, color (e.g., red, blue, green and optionally alpha), and normal components of these triangles are typically represented as floating point numbers. In that he also teaches handling floating point Z-buffer. The Z-values correspond to vertices of a given primitive being processed within a graphic pipeline. The Z-values received by the pipeline are

Art Unit: 2672

represented in a floating point format which includes a mantissa portion and an exponent portion. Therefore, having the combined teaching of Rossin and Deering as a whole, one of ordinary skill in the art would have found it obvious to modify the floating point operations of Rossin to have a processor for performing geometric calculations on a plurality of vertices of a primitive as claimed. Doing so would enable the Z-values being represented more efficiently resulting in increased performance for the graphics pipeline (col. 10, line 60 to col. 11, line 63; figs. 7-8 and 11).

Re claim 2, Rossin discloses rasterization circuit performs scan conversion on vertices having floating point values (col. 2, lines 12-67). In other words, Rossin teaches three-dimensional transformation, texture mapping, lighting, clipping, and perspective divide operations as well as plane equation generation performed in floating point format.

Re claim 3, Deering discloses a texture circuit coupled to the rasterization circuit that applies a texture to the primitive, wherein the texture is specified by floating point values and a texture memory coupled to the texture circuit that stores a plurality of textures in floating point values (figs. 7-8).

Re claim 5, Rossin discloses the floating point format is comprised of sixteen bits (col. 1, lines 32-44). Rossin teaches floating point values have 16 bits.

Re claim 7, Rossin discloses a lighting circuit coupled to the rasterization circuit for performing a lighting function, wherein the lighting function executes on floating point values (col. 2, lines 42-67).

Re claims **6, 8-13 and 22**, the limitations of claims 8-11 and 22 are analyzed as discussed with respect to claim 1.

Re claim **26**, Deering discloses the steps of writing, storing, and reading the data in the frame buffer in the floating point format are further comprised of specifying the floating point format according to a specification, wherein the specification corresponds to a level of range and precision (col. 10, line 51 to col. 11, line 27; col. 8, lines 15-30).

Re claims **32-33 and 35**, Deering discloses the floating point color values are written to, read from, and stored in the frame buffer (col. 10, lines 44-59). In other words, Deering teaches the frame buffer interface comprises logic necessary to read and write pixels from the 3DRAM memories. The frame buffer interface manages the level 1 and level 2 caches (i.e. store data) in the 3DRAM chips.

Re claims **36-37**, Deering discloses the floating point color values are comprised of 16 bits of data and the data are comprised of one sign bit, ten mantissa bits, and five exponent bits (col. 12, line 6 to col. 14, line 65).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the

Art Unit: 2672

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thu Thao Havan whose telephone number is (703) 308-7062. The examiner can normally be reached on Monday to Thursday from 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (703) 305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Thu-Thao Havan
July 8, 2004



MATTHEW LUU
PRIMARY EXAMINER